INTEGRATION METHOD OF A SEMICONDUCTOR DEVICE HAVING A RECESSED GATE ELECTRODE

TECHNICAL FIELD

This disclosure relates to an integration manufacturing method of a semiconductor memory device such as a Dynamic Random Access Memory (DRAM), and, more specifically, to a method to produce DRAM cells having a recessed gate and a planer gate electrode.

BACKGROUND

Integrated circuits, such as ultra-large scale integrated (ULSI) circuits, can include as many as one billion transistors or more. Most typically, ULSI circuits are formed of Field Effect Transistors (FETs) formed in a Complementary Metal Oxide Semiconductor (CMOS) process. Each MOSFET includes a gate electrode formed over a channel region of the semiconductor substrate, which runs between a drain region and source region. To increase the device density and operation speed of the integrated circuits, the feature size of transistor within the circuits must be reduced. However, with the continued reduction in device size, sub-micron scale MOS transistors have to overcome many technical challenges. As the MOS transistors become narrower, that is, their channel length decreases, problems such as junction leakage, source/drain breakdown voltage, and data retention time become more pronounced.

One solution to decrease the physical dimension of ULSI circuits is to form recessed gate or "trench-type" transistors, which have a gate electrode buried in a groove formed in a semiconductor substrate. This type of transistor reduces short channel effects by effectively lengthening the effective channel length by having the gate extend into the semiconductor substrate. An example of a portion of a combined ULSI circuit including a standard transistor and a recessed gate transistor is illustrated in FIG. 1. However, effectively forming recessed gate transistors in ULSI circuits that also contain non recessed gate transistors has been a difficult task.

Embodiments of the invention address these and other problems in the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention, which,

however, should not be taken to limit the invention to the specific embodiments, but are to facilitate explanation and understanding.

FIG.1 is a cross-sectional diagram of a MOSFET having a recessed gate according to the prior art.

FIGs. 2, 3, 4, 5A, 6A and 7A are cross-sectional diagrams of a method of forming a MOSFET with a recessed gate and a planer gate electrode according to an embodiment of the present invention.

FIGs. 5B and 6B are cross-sectional diagrams illustrating alternative processes that were illustrated in FIGs 5A and 6A, respectively.

FIG 7B is a cross-sectional diagram illustrating another alternative process that was illustrated in FIGs 7A.

Figs. 8 to 12 are cross-sectional diagrams illustrating a method of forming a MOSFET having a recessed gate and a planer gate electrode according to another embodiment of the present invention.

Figs. 13 to 17 are cross-sectional diagrams illustrating a method of forming a MOSFET having a recessed gate and a planer gate electrode according to yet another embodiment of the present invention.

Figs. 18 to 22 are cross-sectional diagrams illustrating of a method of forming a MOSFET having a recessed gate transistor in a cell region and a recessed gate in a peripheral region of a semiconductor substrate according to still a further embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION.

In the following detailed descriptions, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

Embodiments of the invention can provide, compared to conventional memory circuits, an increase in effective channel length, a decrease in channel dosing, and improved qualities in junction leakage and data retention time in a memory circuit that includes at least two types of transistors on a single substrate: transistors having a recessed gate, and transistors having a planer gate electrode.

A manufacturing method of a semiconductor device of an embodiment of the present invention is described with reference to Figs. 2 to 7. As shown in Fig. 2, a semiconductor device according to embodiments of the present invention includes a memory cell array section A and a peripheral circuit section B. The memory cell array section is illustrated in the left-had portion of the figures, while the peripheral circuit section is illustrated in the right-hand portion.

An isolation region 15 is formed on a silicon substrate 10. A thin pad oxide film 18 is formed on the isolation 15 and over an active region in the memory cell array section. An etch stopper layer 20 is formed on the pad oxide film 18. The etch stopper layer 20 is preferably made of nitride, for example SiN, with a thickness of about 100 to 200 angstroms. A first oxide layer 25 is formed on the etch stopper layer 20. The first oxide layer 25 can be formed to a thickness of approximately 1000 angstroms in some embodiments.

A recess mask, for forming the recessed gates for the memory cells is formed in a photoresist layer 30 by conventional photolithography and etching processes. As shown in Fig. 3, a recess gate hole 28 is formed in the memory cell side of the substrate 10 by etching the first oxide layer 25, the pad oxide 18, and the etch stopper layer 20. On the peripheral side of the substrate 10, the first oxide layer 25, the pad oxide 18, and the etch stopper layer are all removed.

As shown in Fig. 4, a gate oxide 35 is formed on the silicon substrate 10 and within the recess holes 28. A gate electrode layer is formed on the gate oxide 35. The gate electrode layer is formed as a two layer structure including a lower gate electrode poly layer 40 and an upper gate electrode layer 45, which could be, for example, Wsi. Next, a gate mask layer 50 is formed on the upper gate electrode layer 45. As shown in Fig. 5A, the gate electrode is completed by performing conventional photolithography and etching processes on the gate mask layer 50, the upper gate electrode 45, and the gate oxide layer 35.

Next, as illustrated in Fig. 6A, a deposited insulating layer is etched back to form a spacer 60. Finally, as illustrated in Fig. 7A, a Cosi (Cobalt-Silicon) layer 70 is formed on the peripheral circuit region. The Cosi layer 70 reduces sheet resistance in the peripheral region.

Some alternative methods for forming the memory circuit according to embodiments of the invention are illustrated in FIGs 5B, 6B, and 7B. As shown in Figs. 5B and 6B, the first oxide layer 25 and gate oxide 35 are removed from areas other than under the gate stack in the cell region (FIG. 5B), and gate stack spacers 60 are formed around the gate stack (FIG 6B). FIG. 6B is similar to FIG. 6A, except for the removed oxide layer 25, etch stopper layer

20 and pad oxide layer 18. FIG. 7B shows that another alternative embodiment is to add the spacers 60 before etching the oxide layer 25, etch stopper layer 20 and pad oxide layer 18.

Another embodiment of forming a semiconductor memory device is illustrated in FIGs. 8-12. As shown in Fig. 8, a semiconductor device according to embodiments of the present invention includes a memory cell array section A and a peripheral circuit section B. An isolation region 15 is formed on a silicon substrate 10. A thin pad oxide film 18 is formed on the isolation 15 and over an active region in the memory cell array section. An etch stopper layer 20 is formed on the pad oxide film 18. The etch stopper layer 20 is preferably made of nitride, for example SiN, with a thickness of about 100 to 200 angstroms. A first oxide layer 25 is formed on the etch stopper layer 20.

A recess mask for forming the recessed gates for the memory cells is formed in a photoresist layer 30 by conventional photolithography and etching processes. As shown in Fig. 9, a recess gate hole 28 is formed in the memory cell side of the substrate 10 by wet etching the first oxide layer 25, the etch stopper layer 20, and the pad oxide layer18. As shown in Fig. 10, a gate oxide 35 is formed on the silicon substrate 10 and within the recess holes 28. A gate electrode having a two layer structure formed of a lower gate electrode poly 40 and an upper gate electrode Wsi 45 is formed on the gate oxide 35. A gate mask layer 50 is formed on the Wsi layer. As compared to FIG. 4, described above, FIG. 10 illustrates that the lower gate electrode layer 40, the upper gate electrode Wsi layer 45, and the gate mask layer 50 are all at even levels in both the peripheral area and the cell area of the semiconductor substrate 10.

As shown in Fig. 11, a gate electrode is formed by conventional photolithography and etching processes. Next, as illustrated in FIG. 12, a spacer 60 is formed that covers the gate structures in the cell area and the peripheral area of the semiconductor substrate 10.

A further embodiment of forming a semiconductor memory device is illustrated in FIGs. 13 - 17. As shown in Fig. 13, a semiconductor device according to embodiments of the present invention includes a memory cell array section A and a peripheral circuit section B. An isolation region 15 is formed on a silicon substrate 10. A thin pad oxide film 18 is formed on the isolation 15 and over an active region in the memory cell array section. An etch stopper layer 20 is formed on the pad oxide film 18. The etch stopper layer 20 is preferably made of nitride, for example SiN, with a thickness of about 100 to 200 angstroms. A first oxide layer 25 is formed on the etch stopper layer 20. The first oxide layer 25 is formed thicker than illustrated in FIGs 2 and 8, and is formed to a height roughly equal to the height of a gate stack in the peripheral region of the substrate 10.

A photoresist layer 30 is formed over the first oxide layer 25. Next, a recess mask for forming the recessed gates for the memory cells and for forming a planer gate hole 29 (FIG. 14) is formed in a photoresist layer 30, by conventional photolithography and etching processes. Then, the recess gate hole 28 is formed in the first oxide layer 25, etch stopper layer 20, and the pad oxide layer 18, as well as the silicon substrate 10. Additionally, the planer gate hole 29 is formed in the first oxide layer 25 on the peripheral portion of the substrate 10 by an etching process.

The first oxide layer 25 on the peripheral side of the substrate 10 is thicker than the first oxide layer 25 on the cell region portion of the substrate 10.

Next, as shown in FIG. 15, a gate oxide 35 is formed by oxidation process on the substrate 10 and within the recess hole 28 and planer hole 29. A gate electrode stack having a two layer structure is then formed on the gate oxide 35. The gate electrode stack is formed of a lower gate electrode poly layer 40 and an upper gate electrode Wsi layer 45.

As illustrated in FIG. 16, a gate layer mask 50 is formed on the Wsi layer within the recess hole 28 and the planer hole 29. Then, the first oxide layer 25 is removed in areas not covered by the gate layer mask 50 by, for example, a wet etch process. Finally, as illustrated in FIG. 17, spacers 60 are formed on the gate stacks in the cell region and in the peripheral region of the semiconductor substrate.

Yet further methods to form a semiconductor memory device are illustrated in FIGs. 18 - 22. As shown in Fig. 18, a semiconductor device according to embodiments of the present invention includes a memory cell array section A and a peripheral circuit section B. An isolation region 15 is formed on a silicon substrate 10. A thin pad oxide film 18 is formed on the isolation 15 and over an active region in the memory cell array section. An etch stopper layer 20 is formed on the pad oxide film 18. The etch stopper layer 20 is preferably made of nitride, for example SiN, with a thickness of about 100 to 200 angstroms.

A first oxide layer 25 is formed on the etch stopper layer 20. Next, a recess mask 30 is formed by conventional photolithography and etching processes. As shown in Fig. 19, a recess gate hole 28 is formed by etch process in the memory cell region and in the peripheral region of the substrate 10. Next, as shown in Fig. 20, a gate oxide 30 is formed by, for example, an oxidation process in the recess holes 28.

As illustrated in FIG. 20, a gate electrode layer is formed on the gate oxide 35. The gate electrode layer of FIG. 20 has a two layer structure formed of a lower gate electrode poly 40 and an upper gate electrode Wsi 45. In this embodiment, the lower gate electrode poly 40

extends into the recessed gate holes in the cell region and in the peripheral region of the substrate 10. A gate mask layer 50 is formed on the Wsi layer.

As shown in Fig. 21, a set of gates is formed by conventional photolithography and etching processes in the cell region and the peripheral region. Finally, as illustrated in FIG. 22, a spacer 60 is formed by, for example, an etch back process.

As described above in detail, in embodiments of the present invention, a recessed gate cell and a planer gate electrode are simultaneously formed in the same photolithography step. This allows memory circuits to be developed so that the manufacturing processes will be reasonable without increasing the number of the photolithography steps.

Those skilled in the art recognize that the method of forming integrated circuits described herein can be implemented in many different variations. Therefore, although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appending claims without departing from the spirit and intended scope of the invention